

Amendments to the Specification:

Please replace Paragraph [0053] with the following context:

5 As shown in Fig.16, a patterned photo resist layer 340_350 is formed over the semiconductor substrate 10. The photo resist layer 340_350 masks the low voltage device area 120 and has a plurality of openings 350a, 350b, 350c, and 350d exposing a portion of the high voltage device area 110. The exposed portions of the high voltage device area 110 through the openings 350a, 350b, 350c, and 350d are those areas to be
10 heavily implanted with N type or P type dopants. Thereafter, using the patterned photo resist layer 340_350 as an etching mask, the high voltage gate oxide layer 160 is etched through the openings 350a, 350b, 350c, and 350d. The photo resist layer 340_350 is then removed.

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